Remarks

In the present paper, claims 9, 14, 16, and 30-38 have been cancelled, claims 1, 4, 15, 17, 21, 22, 23, 25, 27 and 28 have been amended and new claims 39-50 have been added.

Support for the amendments herein can be found, for example, in the claims as originally filed, and in the specification at page 10, line 25-page 11, line 10; page 15, lines 19-23; page 17, lines 19-27; page 24, lines 8-17; Table 1, starting on page 25 and otherwise throughout the specification and Figures.

No new matter is believed to have been added by the amendments herein. Moreover, since 12 dependent claims were canceled and 12 new dependent claims have been added, no fee is believed to be required.

Allowable Subject Matter

The applicants would like to thank the Examiner for the early indication of allowable subject matter in dependent claims 8-13, 25, 27 and independent claim 29. However, the applicants have not rewritten claims 8-13, 25, 27 into independent form at this time because the applicants believe that the base claims, as amended herein, are patentable over the cited art as set out in greater detail below.

Claim rejections - 35 U.S.C. §103

Claims 1, 3-4, 19, 21, 23-24, and 26 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Japanese Pat. No. JP 4-317254 to Kaneko, (hereinafter, '*Kaneko'*) in view of U.S. Pat. No. 6,819,351 to O'Hara et al. (hereinafter, '*O'Hara*'). According to the MPEP §706.02(j), to establish a *prima facie* case of obviousness, the prior art reference must teach or suggest all the claim limitations[1]. It is the applicants' position that a *prima facie* case of obviousness has not been established for the claims as amended herein. Of the rejected claims, claims 1 and 21 are in independent form.

[1] See also, *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143 - § 2143.03

Claim 1:

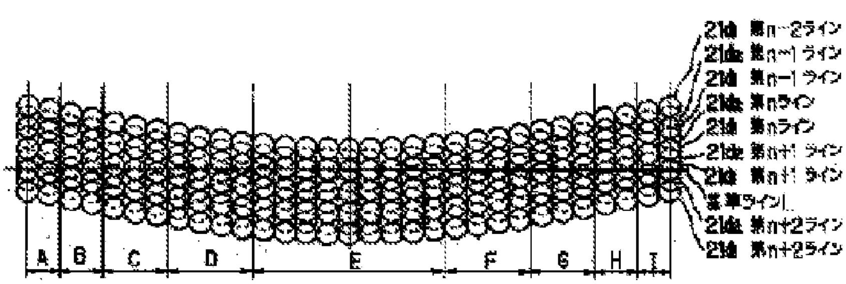
With regard to claim 1, as amended herein, the applicants respectfully assert that neither *Kaneko* nor *O'Hara*, whether taken separately or in combination, disclose, teach or suggest at least:

> A method of electronically adjusting an image to compensate for laser beam process direction position errors … comprising:
> … performing pixel shifts on select columns of said image data based upon a bow profile … wherein said bow profile comprises an instruction for each column of said image data indicating whether that column should be shifted up, down, or not shifted with respect to an adjacent column position …

To the contrary, as conveyed to the Examiner in the interview, both *Kaneko* and *O'Hara* utilize time delays to create absolute line shifts (line increment delays) from a current line position as image data flows to the print driver. The cited references are silent with regard to, and completely fail to teach or suggest, even when combined, an instruction indicating whether a column should be shifted up, down, or not shifted with respect to an adjacent column position as claimed.

For example, *Kaneko*.discloses a controller for adjusting image data communicated to a printhead of a printer for correcting image defects. The correction is achieved by creating a *__time delay__* as the image data flows to the laser driver from the memory. In particular, corrections are implemented by partitioning the scan line (data to be printed) into columns or blocks, e.g., A-I spanning across a page as shown in Fig. 3.

【図3】

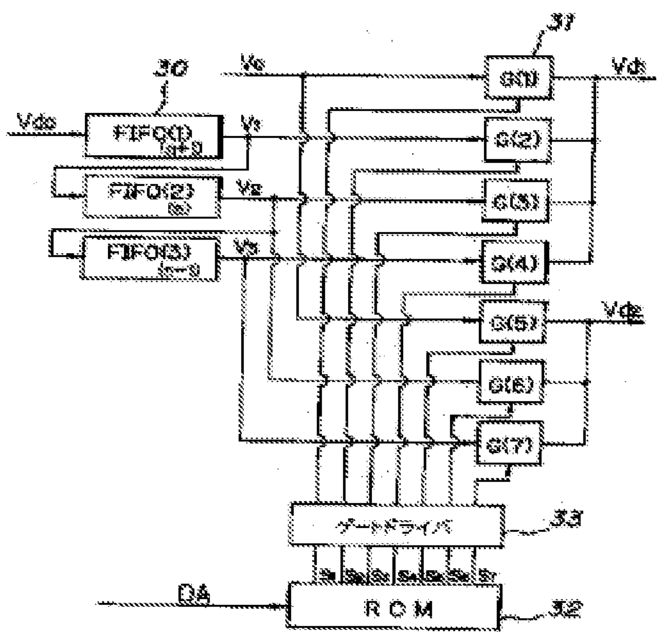


The circuit for effecting the data selection during a given laser beam scan is illustrated in Fig. 8, which is reproduced below. The circuit comprises first, second and third first in, first out (FIFO) memory units, designated FIFO(1)-FIFO(3), and logic gates G(1)-G(7). The output of

the first FIFO, designated V1 represents the input image data Vdo delayed by one scan line. The output V1 is coupled to the second buffer G(2) and cascades into the input of the second FIFO. The output of the second FIFO, designated V2 represents the input image data Vdo delayed by two scan lines. The output V2 is coupled to the third and sixth buffers G(3), G(6) and further cascades into the input of the third FIFO. The output of the third FIFO, designated V3 represents the input image data Vdo delayed by three scan lines. The output V3 is coupled to the fourth and seventh buffers G(4), G(7).

A read only memory (ROM) 32 is provided to set up a division of the main scanning direction and to generate selection signals S1 to S7 for reading data. A gate driver 33 is provided between the ROM 32 and buffers G1-G7.

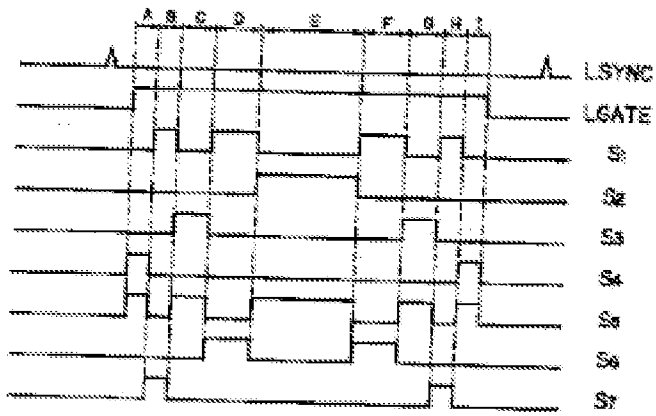
【図8】



From the timing diagram illustrated in Fig. 9, reproduced below, the scan line is aligned by creating whole scan line delays by absolute amounts relative to a designated block. That is, selection signals S4 and S5 are active enabling buffers G4 and G5 when data is to be written for blocks A and I. Selection signals S1 and S7 are active enabling buffers G1 and G7 when data is to be written for blocks B and H; selection signals S3 and S5 are active enabling buffers G3 and G5 when data is to be written for blocks C and G; selection signals S1 and S6 are active enabling

buffers G1 and G6 when data is to be written for blocks D and F; and selection signals S2 and S5 are active enabling buffers G2 and G5 when data is to be written for block E.

【図9】



Kaneko is completely silent with regard to, and fails to teach or suggest a bow profile that comprises an instruction for each column of image data indicating whether that column should be shifted up, down, or not shifted with respect to an adjacent column position as claimed. Rather, control signals are utilized to select, for blocks of column positions at a time, an absolute shift by creating time delays using cascaded line buffers.

The invention in *O'Hara* is conceptually the same as that taught in *Kaneko* for relevant purposes herein. For example, as seen in Fig. 3, correction is accomplished by performing absolute time shifts to selected image data.

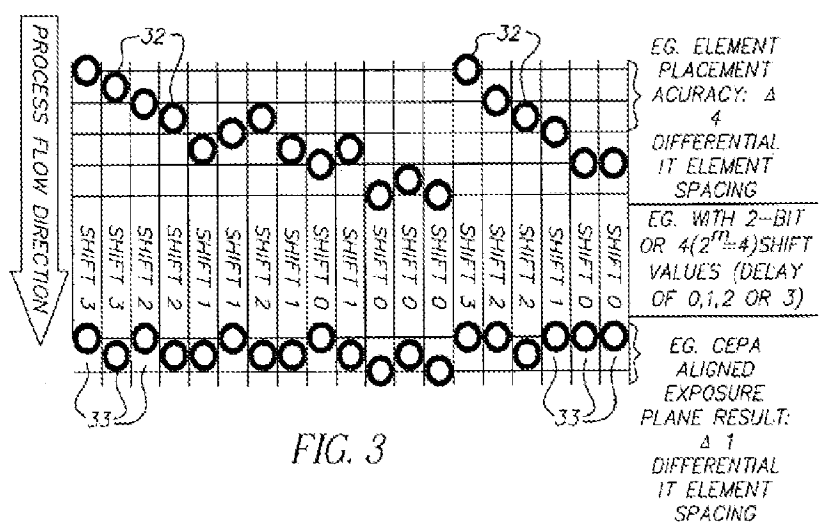


FIG. 3

In particular, a coarse electronic printhead adjustment (CEPA) process uses a determined number of shift values (line delay increments) for each of the LED elements within a corresponding exposure device. The number of line shifts can be scaled by changing the number of bits used to represent the number of line delays. As FIG. 3 illustrates, four unique line shift values are possible (0, 1, 2 or 3) for electronic shifting of data[2]. Thus, *O'Hara* provides finer resolution of correction to the use of blocks in *Kaneko*. However, the approaches are analogous.

That is, the CEPA in *O'Hara* uses a FIFO type system[3] to create time delays based upon absolute offset measurements from the current line of image data as data flows to the print driver during an imaging operation. Moreover, *O'Hara* is completely silent with regard to, and fails to teach or suggest a bow profile that comprises an instruction for each column of image data indicating whether that column should be shifted up, down, or not shifted with respect to an adjacent column position as claimed.

In view of the amendments and clarifying remarks herein, the applicants respectfully request that the rejection of claim 1 and the claims that depend therefrom be withdrawn.

With specific regard to claim 2, as shown above, the corrections taught in *Kaneko* and *O'Hara* utilize cascaded line buffers and registers. However, such disclosure is completely silent with regard to, and fails to teach or suggest that first and second memory locations are areas of a main system memory. To the contrary, the FIFOs used by both *Kaneko* and *O'Hara* serve as time delays as data flows to the corresponding print driver and is explicitly not stored back to main memory.

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[2] See for example, *O'Hara*, Fig. 3, Col. 5, lines 15-39; Col. 5, line 56-Col. 6, line 13.
[3] See also, *O'Hara*, Col. 7, lines 42-51.

Claim 21:

With regard to claim 21, as amended herein, the applicants respectfully assert that neither *Kaneko* nor *O'Hara*, whether taken separately or in combination, disclose, teach or suggest at least:

> A system for electronically adjusting image data … comprising:
>
> …
>
> a bow processor operatively configured to selectively obtain said image data from said main memory location, apply pixels shifts on select columns of said image data and store said adjusted image data wherein:
>
> said bow processor applies pixels shifts on columns of the selected image data based upon a first bow profile that characterizes said first process direction position errors of Pels written by said first laser beam when processing image data associated with said first color image plane to define first adjusted image that is pre-warped in the process direction in a manner corresponding to said first bow profile, said first adjusted image data stored in said first memory location …

To the contrary, as described more fully herein with reference to claim 1, both *Kaneko* and *O'Hara* utilize cascaded line buffers and registers to create time delays as image data flows to the corresponding laser driver. As such, the configurations in *Kaneko* and *O'Hara* can only correct a single image plane using a single correction profile. For example, the same FIFOs cannot be re-used with a completely different bow profile to bow image data associated with a completely different printhead, photoconductive drum or other image plane data. This can be further seen, for example, by noting that in both *Kaneko* and *O'Hara*, the corrections are being performed as the image data flows to the driver circuitry.

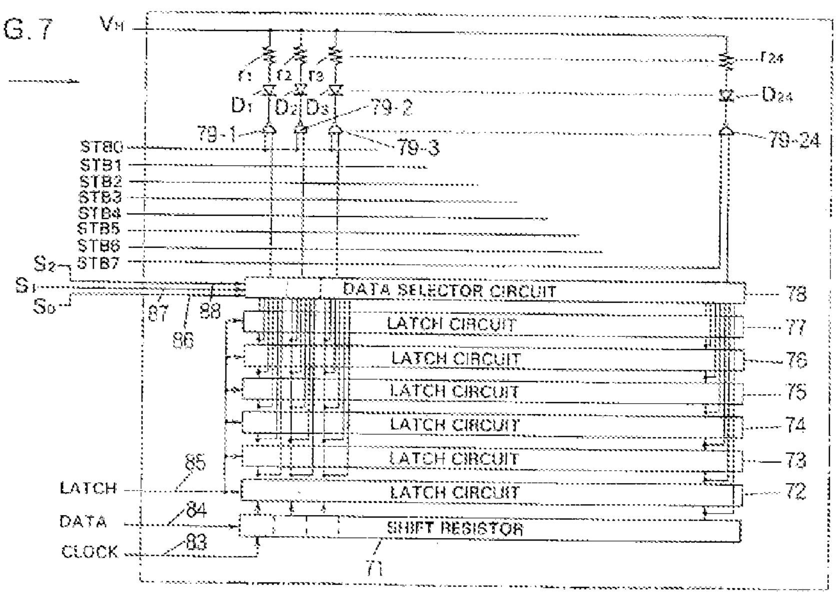
In view of the amendments and clarifying remarks herein, the applicants respectfully request that the rejection of claim 21 and the claims that depend therefrom be withdrawn.

Claims 2, 14-18, 20, and 28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Kaneko* in view of *O'Hara* and further in view of U.S. Pat. No. 5,719,680 to Yoshida et al., (hereinafter, '*Yoshida*').

The applicants assert that these claims are patentable by virtue of depending from a base claim, which applicants believe is patentable over the cited art as described more fully herein.

Moreover, the combination of *Yoshida* with *Kaneko* and *O'Hara* fails to teach or suggest that claimed in claims 1 and 21. In this regard, the applicants note that *Yoshida* is analogous for relevant purposes to both *Kaneko* and *O'Hara*. As seen in Fig. 7, reproduced below, *Yoshida* teaches using lines of pixel data that are cascaded into a series of line buffers 72, 73, 74, 75, 76, 77. A data selector circuit 78 (multiplexer) drives the LEDs D1-D24 of the LED printhead by selecting portions of the line buffers 72-77 based upon control signals S0, S1 and S2[4], the corresponding strobe signals STB0-STB7 and associated NAND gates. In this regard, the system of *Yoshida* is analogous to that taught by *Kaneko*.

FIG.7



Claims 5-7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Kaneko* in view of *O'Hara* in further view of U.S. Pat. No. 6,445,404 to Kerby et al., (hereinafter, '*Kerby*'). In view of the amendments and comments herein, the applicants respectfully request that the rejections to claims 5-7 be withdrawn as these claims depend from claim 1, which applicants believe is patentable as set forth in greater detail above.

[4] See for example, U.S. Pat. No. 5,719,680, Col. 4, lines 1-64.

Claim 22 stands rejected under 35 U.S.C. §103(a) as being unpatentable over *Kaneko* in view of *O'Hara* in further view of U.S. Pat. No. 5,764,243 to Baldwin et al., (hereinafter '*Baldwin*'). In view of the amendments and comments herein, the applicants respectfully request that the rejection to claim 22 be withdrawn as claim 22 depends from claim 21, which is submitted to be patentable as set forth above.

New Claims

Each of the new claims herein depends from a base claim which the applicants believe is patentable as set out more fully herein. In particular, new claims 39-41, which depend from claim 29, recite subject matter that is analogous to pending claims 10-13 which depend from claim 1.

New claims 42-50 depend from claim 1 and recite subject matter analogous to that recited in claims 30-38. Claims 30-38 were previously withdrawn subject to a restriction requirement, but that subject matter is now presented in dependent form.

Conclusion

For all of the above reasons, the applicants respectfully submit that the above claims recite allowable subject matter. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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